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JC857 U.S. PTO
09/941761

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Class Subclass
ISSUE CLASSIFICATION

PATENT NI

U.S. UTILITY Patent Application

APPLICATION NO. 09/941761	CONT/PRIOR	CLASS 438	SUBCLASS	ART UNIT 3811	EXAMINER
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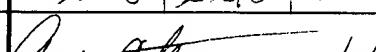
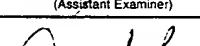
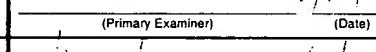
ANSWER

Method and structure for temporarily isolating a die from a semiconductor conductor to facilitate wafer level testing

PTO-2040
12/99

ISSUING CLASSIFICATION

Continued on Issue Slip Inside File Jacket

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	78	12/2	#2	47	1
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____	 Andrew C. Stevens (Assistant Examiner)  John F. Neiburg Supervisory Patent Examiner Serial No. 30-100000 5/16/03 (Primary Examiner) (Date)			NOTICE OF ALLOWANCE MAILED 05/20/03	
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.	 Jennifer L. Dunker Legal Instruments Examiner (Date)			ISSUE FEE Amount Due \$1600 Date Paid 5-20-03	
				ISSUE BATCH NUMBER	

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